## Lathif Sharieff

Embedded Systems Engineer | AI Hardware Enthusiast



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Stuttgart, Germany



Motivated and accomplished young professional with a specialized focus in Digital Design and RTL design, complemented by a robust background in FPGA design. My professional journey is marked by diverse internships and hands-on projects that have equipped me with a profound understanding of AI hardware and Domain-specific Architecture principles.

### **EDUCATION**

Apr 2024 Apr 2021 Master of Science in Embedded Systems Engineering | Universität Freiburg, Germany

> Coursework: Computer Architecture, Artificial Intelligence, Embedded Systems, Hardware Verification, Cyber-Physical Systems, Hardware Security and Testing, Sensors.

Jul 2020 Aug 2016 Bachelors of Engineering in Electronics and Telecommunications | VTU Bengaluru, India

> Coursework: Digital System Design, DSP, Wireless and Mobile Communication, IoT, HDL programming, Embedded Systems Design, Micro-Controllers, VLSI Design, Cryptography.

### Professional Experience

Apr 2024 Oct 2023 Research Assistant (Thesis: DSP Engine for ML Accelerator) | Universität Tübingen, Germany



- > Architected and implemented a high-performance DSP engine, incorporating MFCC extraction architecture for a ML accelerator optimized for audio processing.
- > Engineered a custom FFT core, FIR and Hamming filters for efficient audio processing, and a robust AHB Bus fabric for seamless integration into the ML accelerator (UltraTrail).

Sep 2023 Jun 2023 AI Hardware Engineer | Gemesys, Germany



- > Spearheaded collaboration between software and hardware teams in an agile environment.
- > Optimized Deep Learning models on proprietary neuromorphic hardware using quantization techniques, focusing on accelerating training cycles and maximizing model accuracy.
- > Developed an initial prototype for a proprietary neuromorphic algorithm on Xilinx FPGA tool flow, establishing the framework for future optimization and performance gains.

Mar 2023 Oct 2022 Deep Learning Hardware Engineer (Intern) | Bosch Centre for Artificial Intelligence, Germany



- > Developed the RTL design for the **Neural Computing Engine (NCE)** and AXI (ARM-AMBA) Interface, vital components of the AI IP, resulting in performance enhancements.
- > Executed RTL simulation of the developed IP, utilizing advanced EDA tools and toolchain software, and leveraging scripting skills within Linux and Git-based environments.
- > Contributed to the micro-architecture design of the IP while conducting extensive research and analysis on AI hardware and Domain Specific accelerators.

Sep 2022 Sep 2021

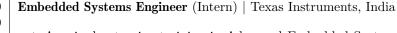


Research Assistant | IMTEK Freiburg, Germany

- > Engineered an electrochemical sensor system on an Arduino Uno board.
- > Tested various samples for cyclic voltammetry with the LPC1343 board, and published a research paper in collaboration with KIT.

Aug 2019 Jun 2019

TEXAS INSTRUMENTS



- > Acquired extensive training in Advanced Embedded Systems and IoT Applications, with a focus on MSP430, ARM Cortex M4 architecture and Industrial applications.
- > Developed and implemented an image recognition project on the BOOSTXL board.

# SKILLS

Programming Languages Verilog, System Verilog, Python, C, VHDL, MATLAB, TCL

Frameworks/Standards UVM, TensorFlow (TFlite)

**Developer Tools** Xilinx Vivado, ModelSim, Quartus, Icarus Verilog, Arduino, Altium

Miscellaneous Git (Version control), Azure (Project management)

**Technologies** ASIC & FPGA workflow, AI accelerators, Neuromorphic computing

Languages English - C1, German - A2 (Actively learning)

Soft Skills Analytical, structured, result-orientated team player and an inclusive and collabora-

tive personality with excellent social and communication skills.

### **PROJECTS**

Deep Learning Accelerator | Verilog, Hardware Acceleration

Developed a scalable FPGA-based Deep Learning Accelerator Unit featuring three pipelined processing units. This design leverages matrix multiplication, tiling techniques, and FIFO buffers to enhance throughput and data locality.

**AES Encryption Engine** | Verilog, Cryptography, ModelSim

Implemented a high-performance AES-128 encryption engine using Verilog, subsequently simulating it on Modelsim

10-port router for NoC | Verilog, Xilinx Spartan-6, ISE design

Spearheaded a team to design a 10-port router for NoC on an FPGA. The project was awarded by IISc, India.

RISC-V processor | Verilog, Processor design, Icarus Verilog

Designed and implemented a single-cycle processor based on RISC-V architecture, utilizing open-source EDA toolchain.

Audio Processing | Verilog, I2S, SPI, I2C, iCEcube

Collaborated with Telocate GmbH to design an audio processing system and managed requirements capture to design verification. Integrated a Lattice FPGA, Audio Codec, MEMS microphone, and multiple communication interfaces.

### CERTIFICATIONS

$ \begin{array}{c} \textbf{Accelerators for Deep Learning} \\ IIT\ Roorkee \end{array} $	Embedded Machine Learning Edge Impulse	$ \begin{array}{c} \textbf{Project Management} \\ Google \end{array} $
$\begin{array}{c} \textbf{Machine Learning Hardware} \\ Cornell \end{array}$	$\begin{array}{c} \textbf{Advanced SoC Design} \\ Arm \end{array}$	$egin{align*} \mathbf{Verilog} \ Udemy \ \end{aligned}$

#### AWARDS AND INTERESTS

- > Awards: STIBET-I scholarship DAAD, VELA Stipendiat Eccelisia group and Maria-Ladenburger scholarship.
- > Interests: Volunteering & Mentoring, Photography, Poetry, Travelling.